UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,699	10/16/2003	Fred Hartnett	200209079-1	9165

22879 7590 08/08/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
TANG, MINH NHUT	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/686,699	HARTNETT ET AL.	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *14-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 14-27 stand withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on July 05, 2005.

2. This application contains claims 14-27 drawn to an invention nonelected with traverse filed on July 05, 2005. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means", "comprise" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because the form and legal phraseology often used in patent claims, such as "comprise", "means" and "said" should be avoided. Correction is required.

5. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, 6, 9-10, 12, 28 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Hartnett et al. (U.S.P. 6,437,587).

As to claim 1, Hartnett et al. discloses, in Figs. 1-4, an electronic circuit assembly test apparatus (10), comprising: a support member (18) having a plurality of probes (22), each probe (22) adapted to contact a corresponding test area of an electronic circuit assembly (12); and a probe assembly (20) coupled to the support member (18), the probe assembly (20) having a plurality of probes (42, Fig. 3) configured to contact test areas of the electronic circuit assembly (12) different than (see, for example, column 4, lines 1-11) the test areas contacted by the probes (22) of the support member (18), wherein a spacing density of the probes (42) of the probe assembly (20) is greater than a spacing density of the probes (22) of the support member (18, see column 3, lines 47-56).

As to claim 2, Hartnett et al. discloses in column 3, lines 12-16, the spacing density of the probes (42) of the probe assembly (20) corresponds to test areas of an integrated circuit.

As to claims 6 and 32, Hartnett et al. discloses in Figs. 1-4, the probe assembly (20) is movably (i.e., for making electrical contact with pads 34) coupled to the support member (18) to provide non-lateral movement of the probe assembly (20) relative to the support member (18).

As to claim 9, Hartnett et al. discloses, in Figs. 1-4, an electronic circuit assembly test apparatus (10), comprising: first probe means (22) coupled to a support member (18) and adapted to contact corresponding test areas on an electronic circuit assembly (12); support means (20) coupled to the support member (18); and second probe means (42) coupled to the support means (20) and configured to contact test areas on the electronic circuit assembly (12) different than (see, for example, column 4, lines 1-11) the test areas contacted by the first probes means (22), the second probe means (42) having a spacing density of probes greater than a spacing density of probes of the first probe means (22, see column 3, lines 47-56).

As to claim 10, Hartnett et al. discloses in Figs. 1-4, the support means (20) is movably (i.e., for making electrical contact with pads 34) coupled to the support member (18).

As to claim 12, Hartnett et al. discloses in column 8, lines 12-20, means (alignment devices and machines) for aligning the second probe means (42) with corresponding test areas of the electronic circuit assembly (12).

As to claim 28, Hartnett et al. discloses, in Figs. 1-4, an electronic circuit assembly test apparatus (10), comprising a support member (18) having a plurality of probes (22) configured to contact a first plurality of test areas of an electronic circuit

assembly (12); and a probe assembly (20) coupled to the support member (18), the probe assembly (20) having a plurality of probes (42) configured to contact a second plurality of test areas of the electronic circuit assembly (12), wherein the probes (42) of the probe assembly (20) are spaced to accommodate a spacing density of the second plurality of test areas greater than a spacing density of the first plurality of test areas (see column 3, lines 47-56).

8. Claims 1-2, 6-7, 9-10, 28 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Kocher (U.S.P. 6,292,004).

As to claim 1, Kocher discloses, in Figs. 2 and 8-9, an electronic circuit assembly test apparatus (10), comprising: a support member (14 associated with plates 12, 16a-16d) having a plurality of probes (32, 34), each probe (32, 34) adapted to contact a corresponding test area (i.e., test points) of an electronic circuit assembly (i.e., printed circuit board); and a probe assembly (36) coupled to the support member (14 and plates 12, 16a-16d), the probe assembly (36) having a plurality of probes (38) configured to contact test areas (i.e., selected test points of IC package) of the electronic circuit assembly (printed circuit board) different than the test areas (test points) contacted by the probes (32, 34) of the support member (14 and plates 12, 16a-16d), wherein a spacing density of the probes (38) of the probe assembly (36) is greater than a spacing density of the probes (32, 34) of the support member (14 and plates 12, 16a-16d, see abstract, and column 9, lines 1-17).

As to claim 2, Kocher discloses in column 9, lines 1-17, the spacing density of the probes (38) of the probe assembly (36) corresponds to test areas of an integrated

circuit (IC component package).

As to claims 6 and 32, Kocher discloses in column 9, lines 10-11 and column 10, lines 10-17, the probe assembly (36) is movably coupled to the support member (14 and plates 12, 16a-16d) to provide non-lateral movement of the probe assembly (36) relative to the support member (14 and plates 12, 16a-16d).

As to claim 7, Kocher discloses in Figs. 8-9, the probes (38) of the probe assembly (36) comprise spring-biased probes.

As to claim 9, Kocher discloses, in Figs. 2 and 8-9, an electronic circuit assembly test apparatus (10), comprising: first probe means (32, 34) coupled to a support member (14 associated with plates 12, 16a-16d) and adapted to contact corresponding test areas (test points) on an electronic circuit assembly (printed circuit board); support means (36) coupled to the support member (14 and plates 12, 16a-16d); and second probe means (38) coupled to the support means (36) and configured to contact test areas (selected test point of IC package) on the electronic circuit assembly (printed circuit board) different than the test areas (test points) contacted by the first probes means (32, 34), the second probe means (38) having a spacing density of probes greater than a spacing density of probes of the first probe means (32, 34, see abstract, and column 9, lines 1-17).

As to claim 10, Kocher discloses in column 9, lines 10-11 and column 10, lines 10-17, the support means (36) is movably coupled to the support member (14 and plates 12, 16a-16d).

As to claim 28, Kocher discloses, in Figs. 1-4, an electronic circuit assembly test apparatus (10), comprising a support member (14 associated with plates 12, 16a-16d) having a plurality of probes (32, 34) configured to contact a first plurality of test areas (test points) of an electronic circuit assembly (printed circuit board); and a probe assembly (36) coupled to the support member (14 and plates 12, 16a-16d), the probe assembly (36) having a plurality of probes (38) configured to contact a second plurality of test areas (selected test points of IC package) of the electronic circuit assembly (printed circuit board), wherein the probes (38) of the probe assembly (36) are spaced to accommodate a spacing density of the second plurality of test areas (selected test points of IC package) greater than a spacing density of the first plurality of test areas (see abstract, and column 9, lines 1-17).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 3, 8, 11, 29 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartnett et al. (U.S.P. 6,437,587) in view of Aussant et al. (U.S.P. 5,698,990).

As to claims 3, 8, 11, 29 and 33, Hartnett et al. discloses all the limitations in the claims except for the probe assembly is adapted to move laterally relative to the support member with at least one spring disposed between the probe assembly and the support member. Aussant et al. discloses, in Fig. 2, a probe apparatus comprising a probe plate (54) having a plurality of probe (68), a top plate (56), at least one spring assembly (10) disposed between the probe plate (54) and the top plate (56). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the test apparatus of Hartnett et al. by providing a spring between the probe assembly and the support member for laterally relative moving between the probe assembly and the support member as taught by Aussant et al. so that it would add flexibility in test fixture design.

12. Claims 4 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartnett et al. (U.S.P. 6,437,587) in view of Siew et al. (U.S.P. 6,885,205).

As to claims 4 and 30, Hartnett et al. discloses all the limitations in the claims except for the probe assembly comprises at least one alignment guide adapted to cooperate with an alignment guide disposed on the electronic circuit assembly. Siew et al. discloses, in Figs. 3-3 and 3-4, at least one alignment guide (116-3, 166-4 and 169)

adapted to cooperate with an alignment guide (through holes) disposed on the electronic circuit assembly (102). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the apparatus of Hartnett et al. by providing at least an alignment guide as taught by Siew et al. for accurately aligning the circuit board to be tested with the probes of the test apparatus.

13. Claims 5, 13 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartnett et al. (U.S.P. 6,437,587) in view of Potter (U.S.P. 6,028,437).

As to claims 5, 13 and 31, Hartnett et al. discloses all the limitations in the claims except for the probe assembly comprises at least one limiter adapted to limit movement of the probes of the probe assembly toward the electronic circuit assembly. Potter discloses, in Fig. 1, a probe membrane (120) having probes (122) and a limiter (123). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the apparatus of Hartnett et al. by providing a limiter as taught by Potter so that the probes would not driven beyond their elastic limit.

Response to Arguments

14. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha T. Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MINH NHUT TANG
PRIMARY EXAMINER
8/03/06